

FIG. 1

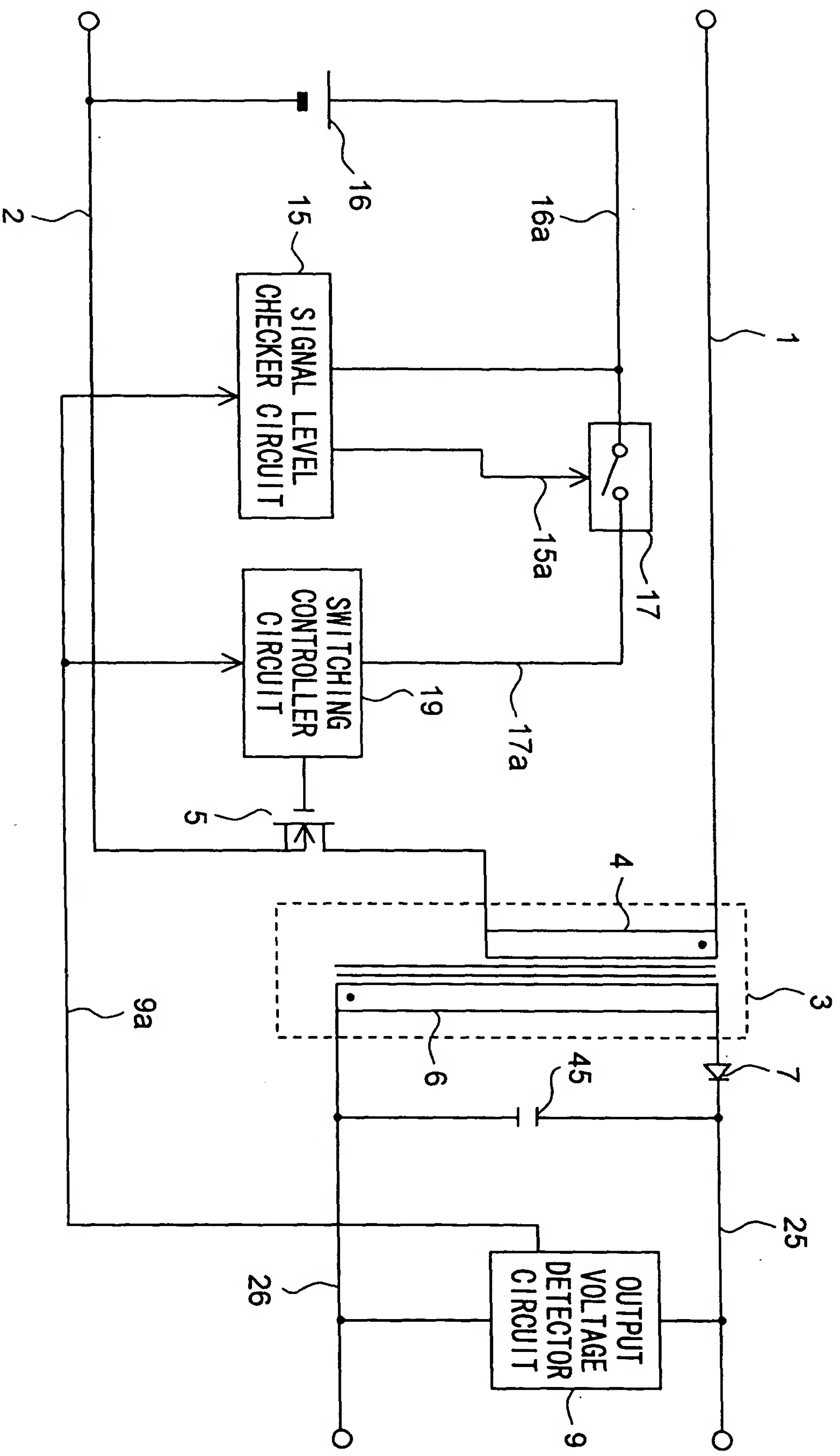
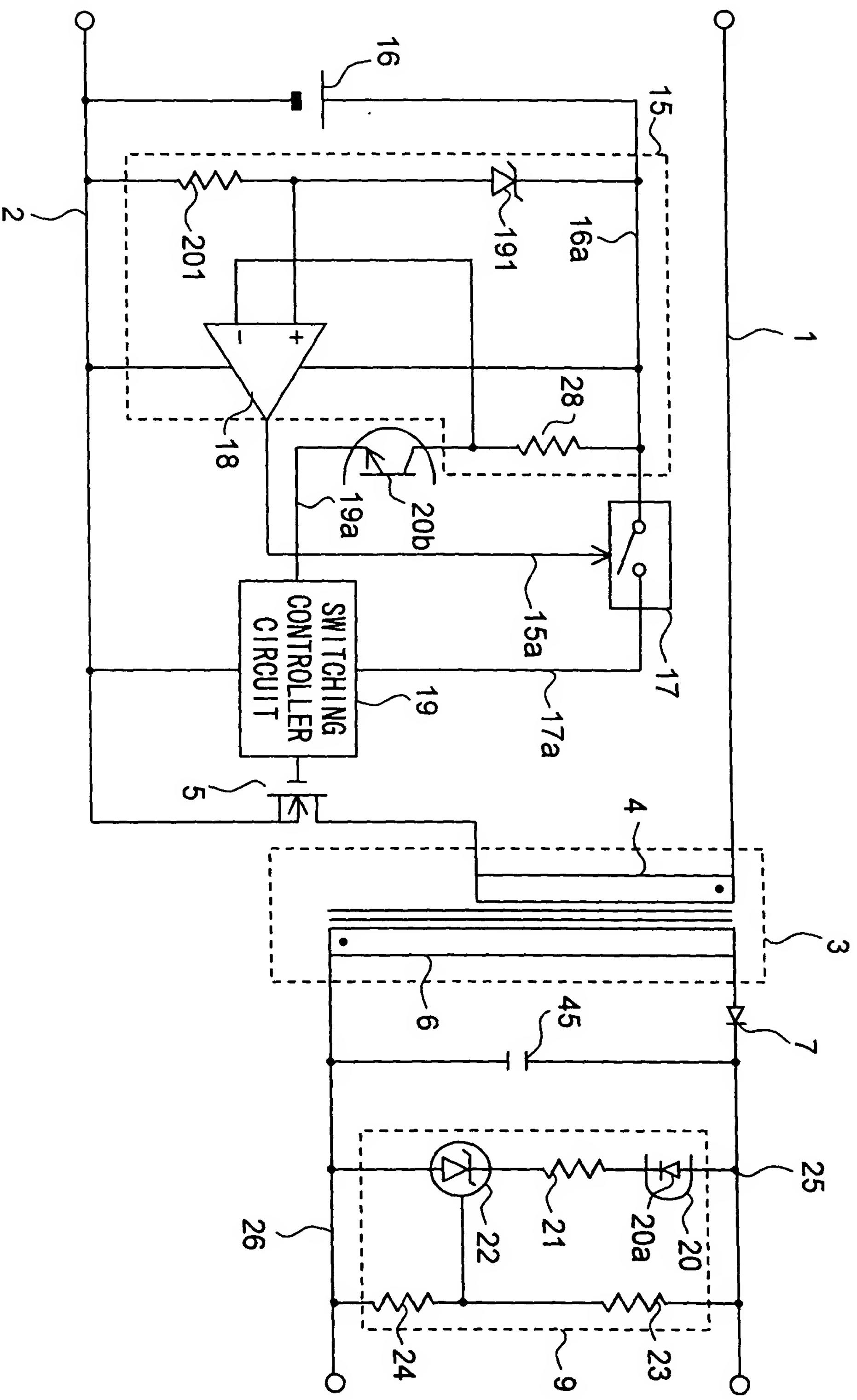


FIG.2



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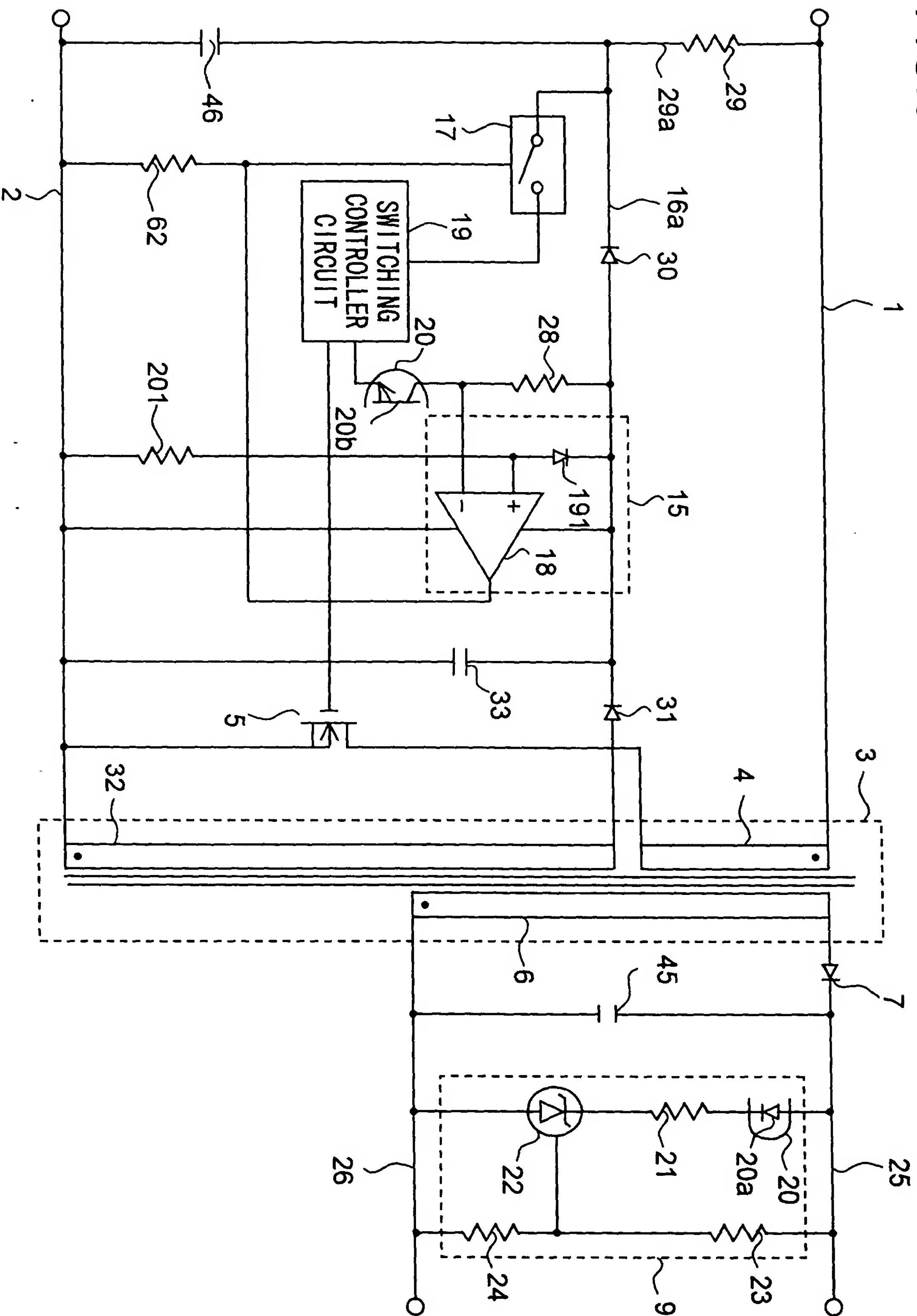


FIG. 4

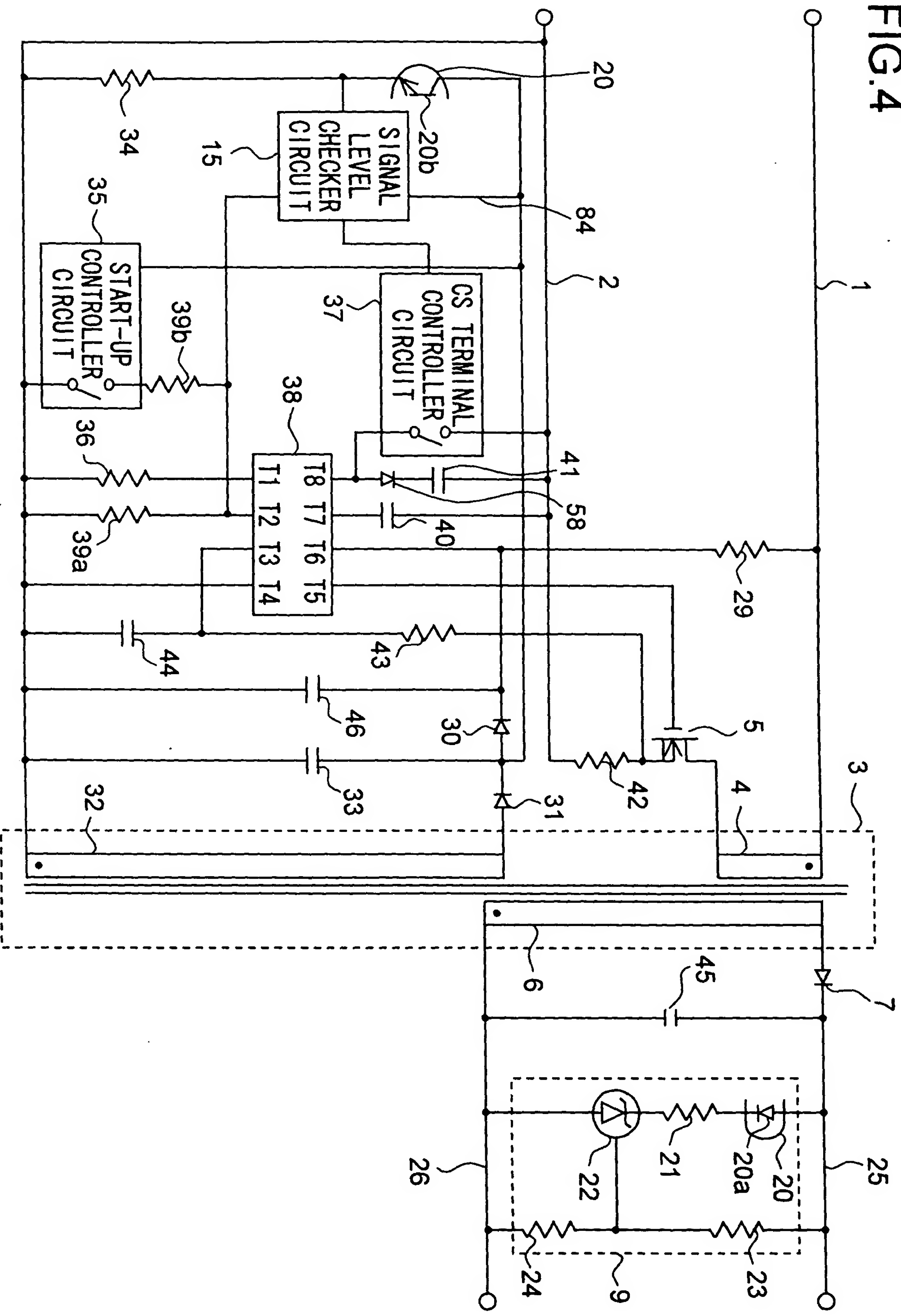


FIG.5

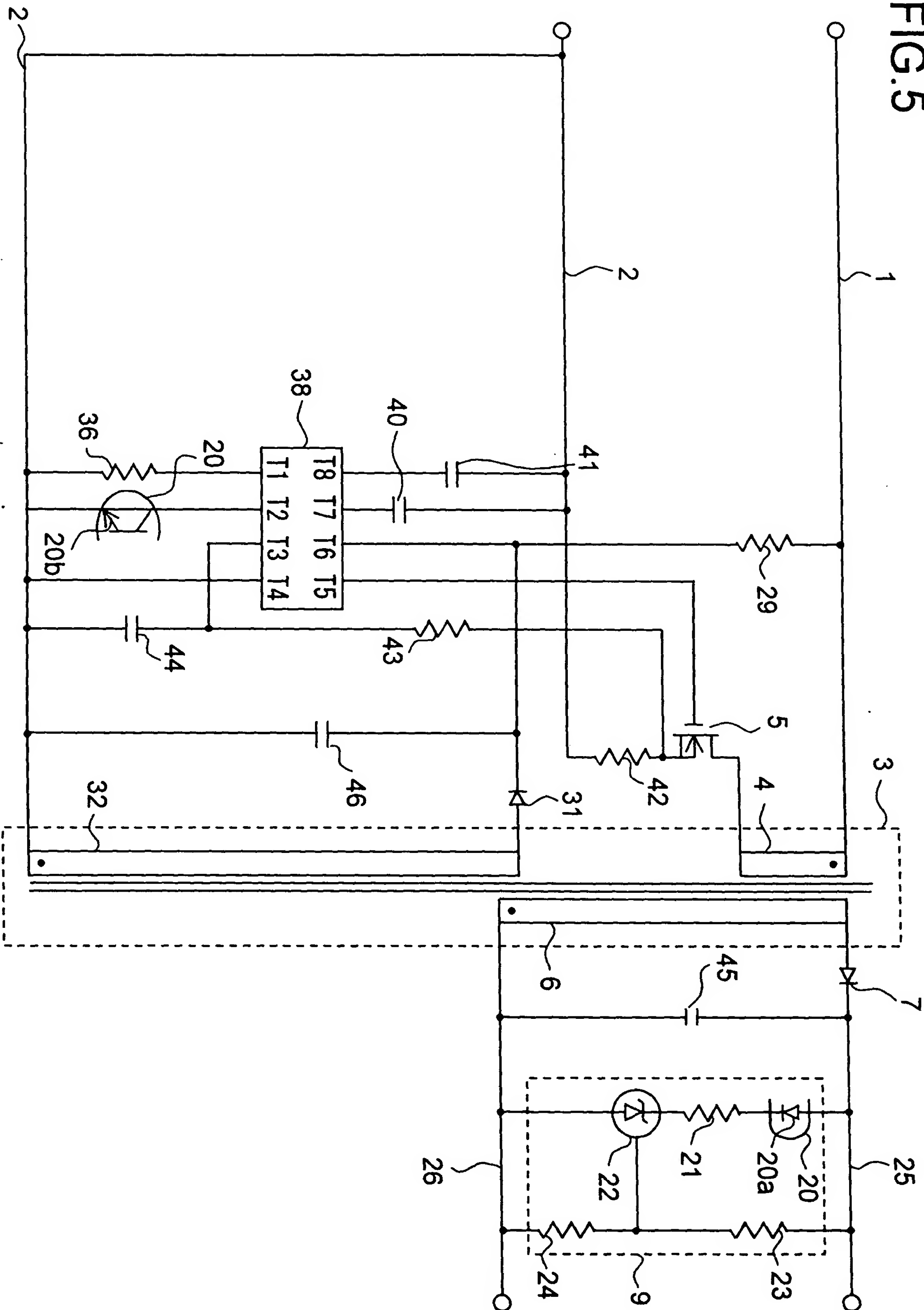


FIG.6

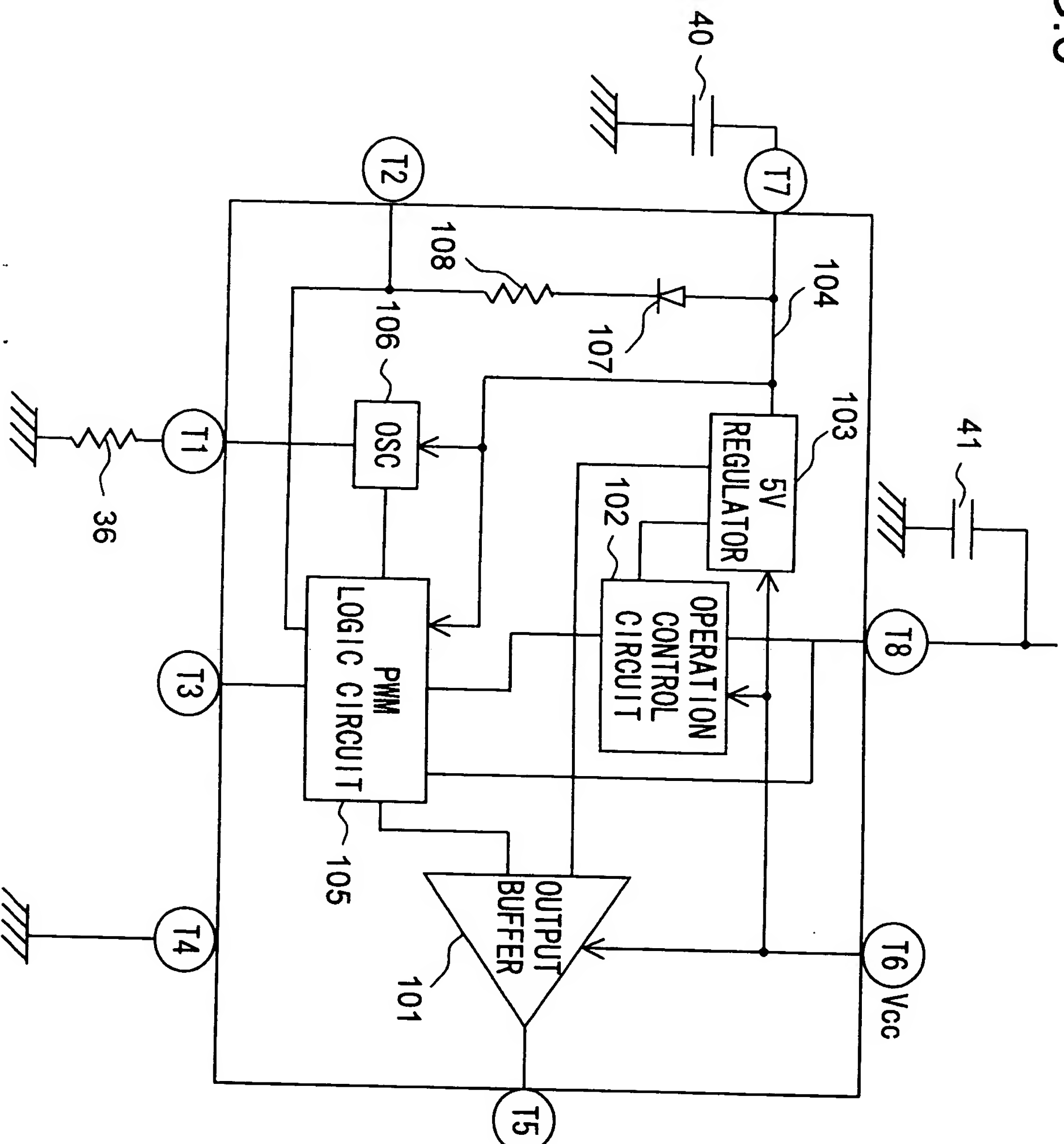


FIG. 7

(a)

(b)

(c)

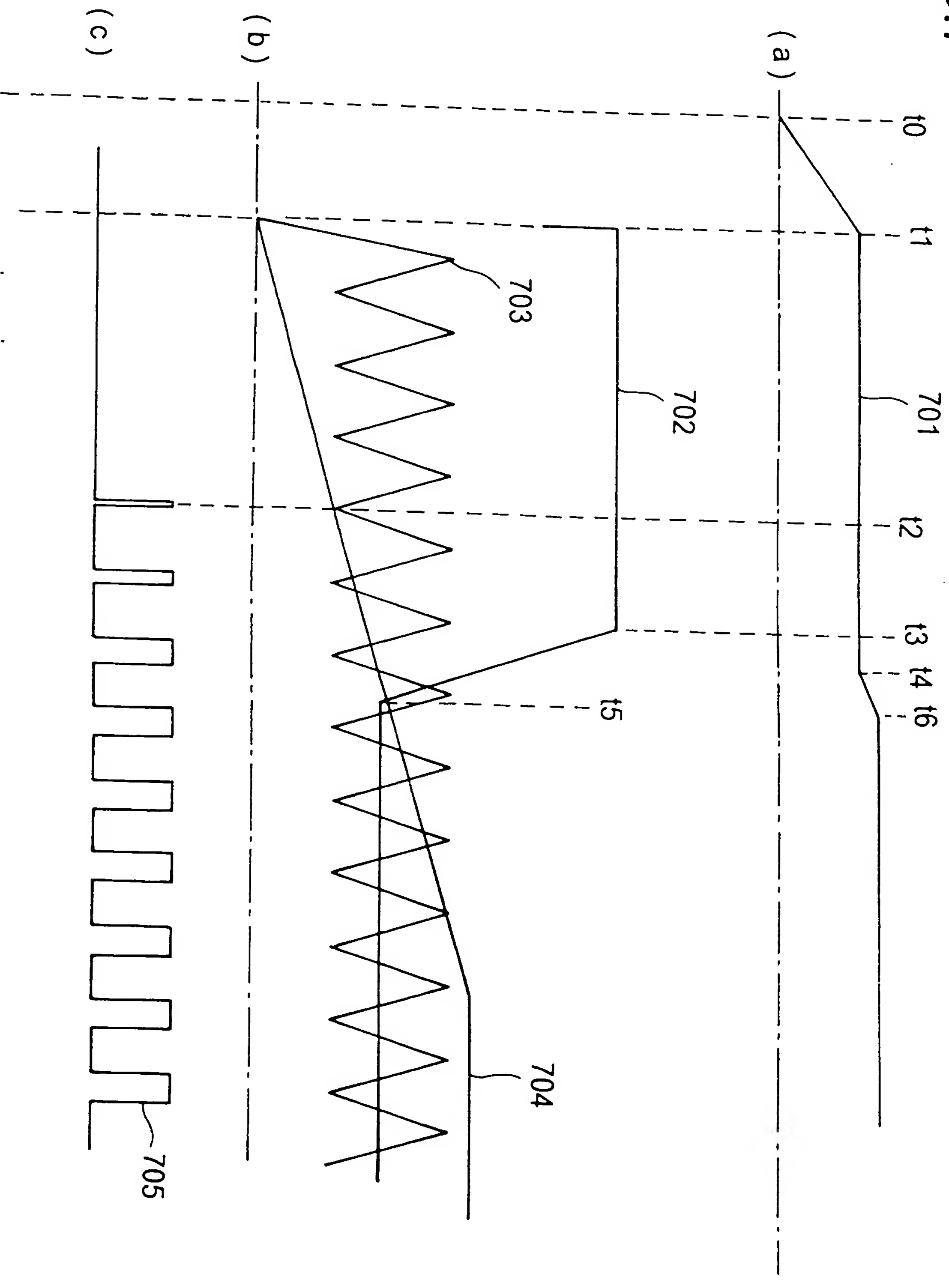


FIG.8

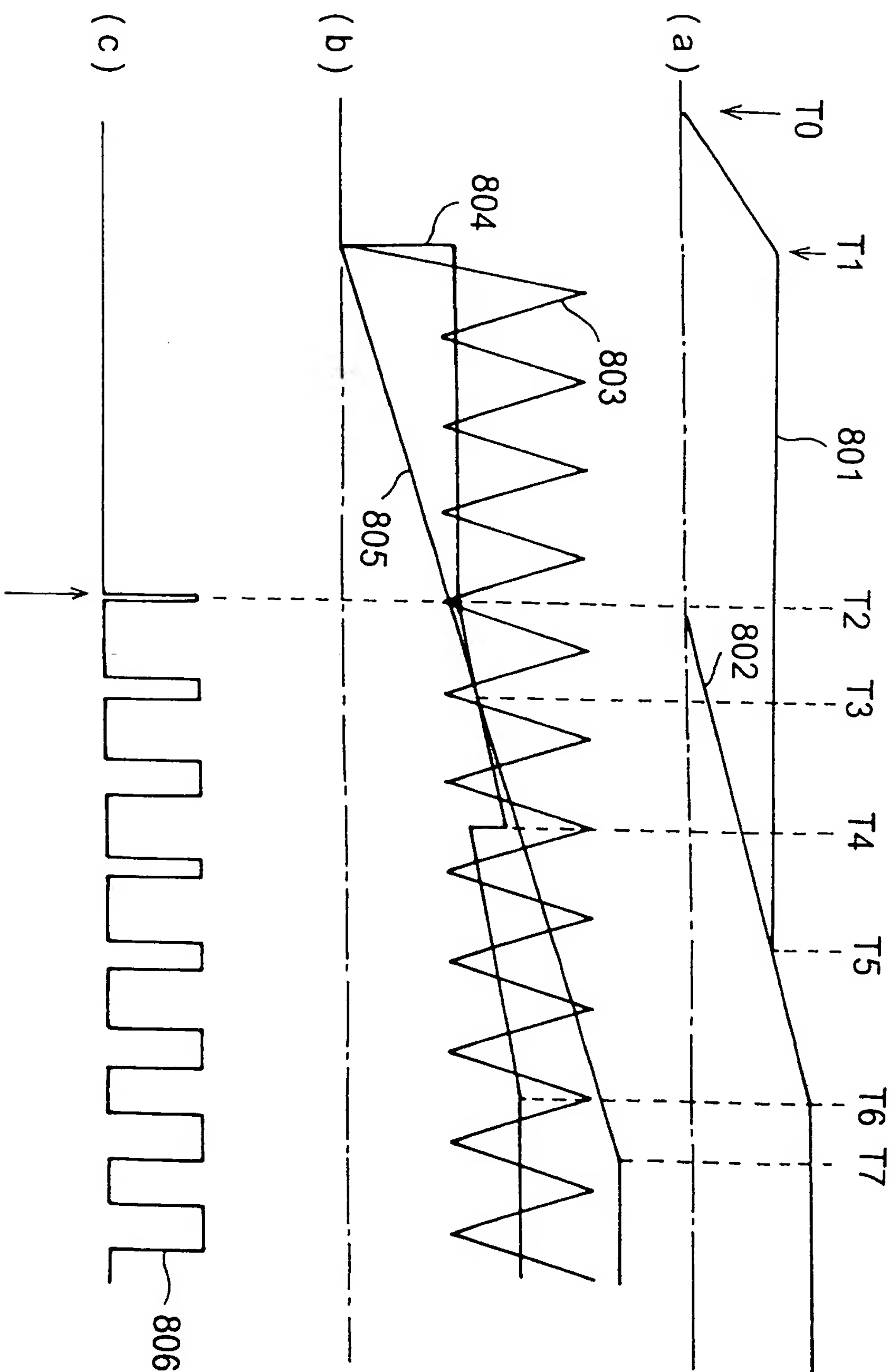


FIG. 9

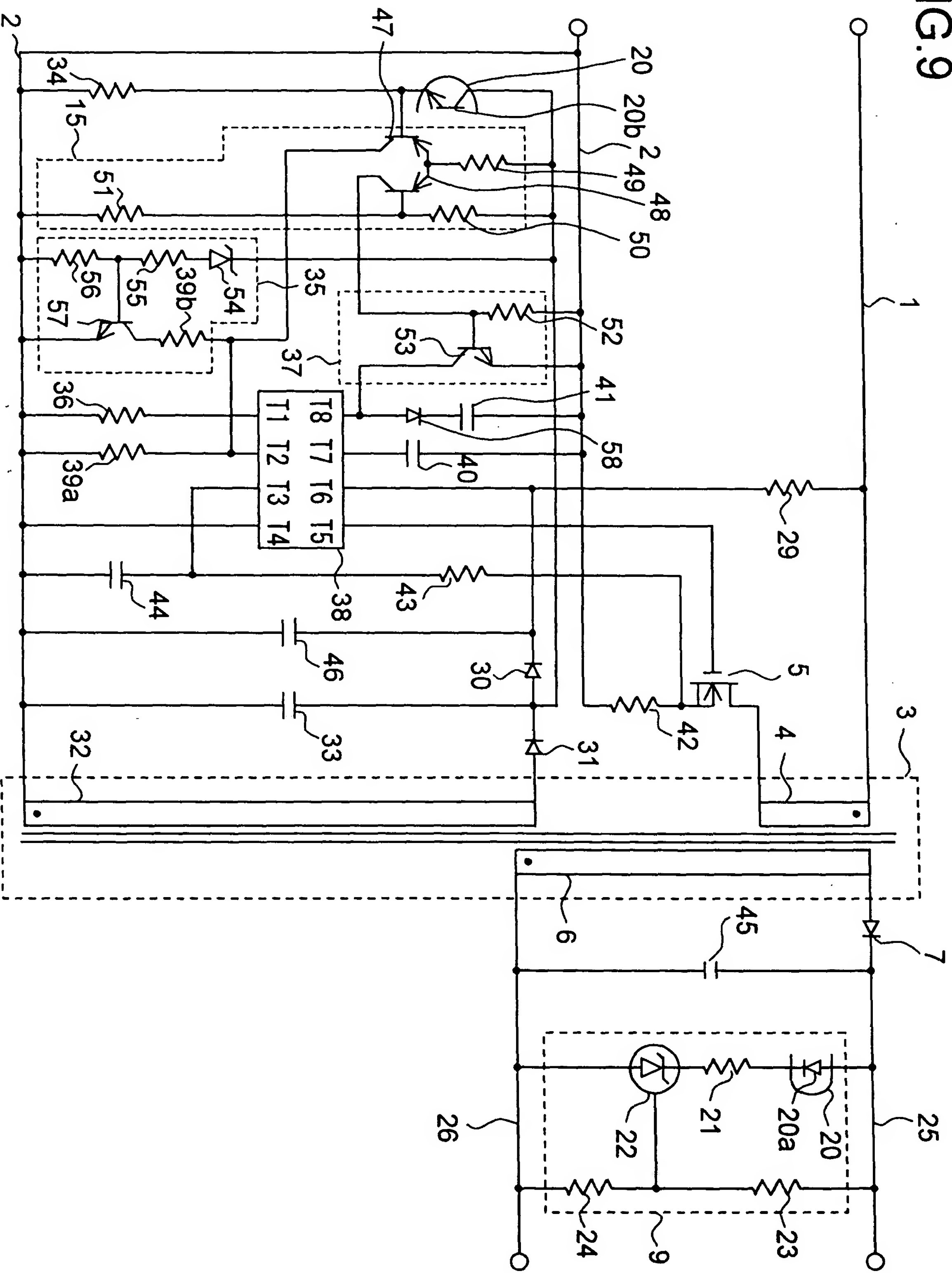


FIG. 10

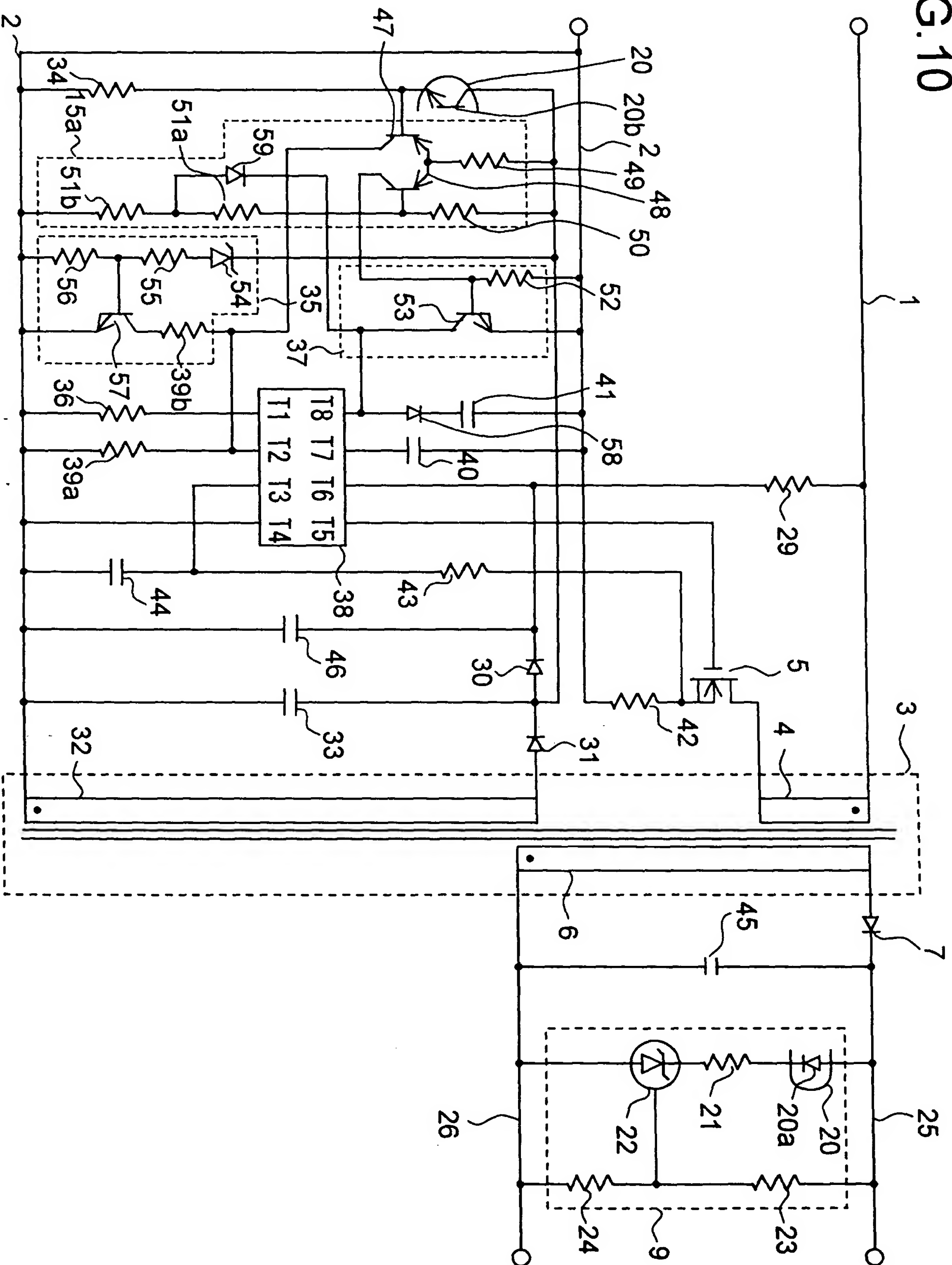


FIG. 11

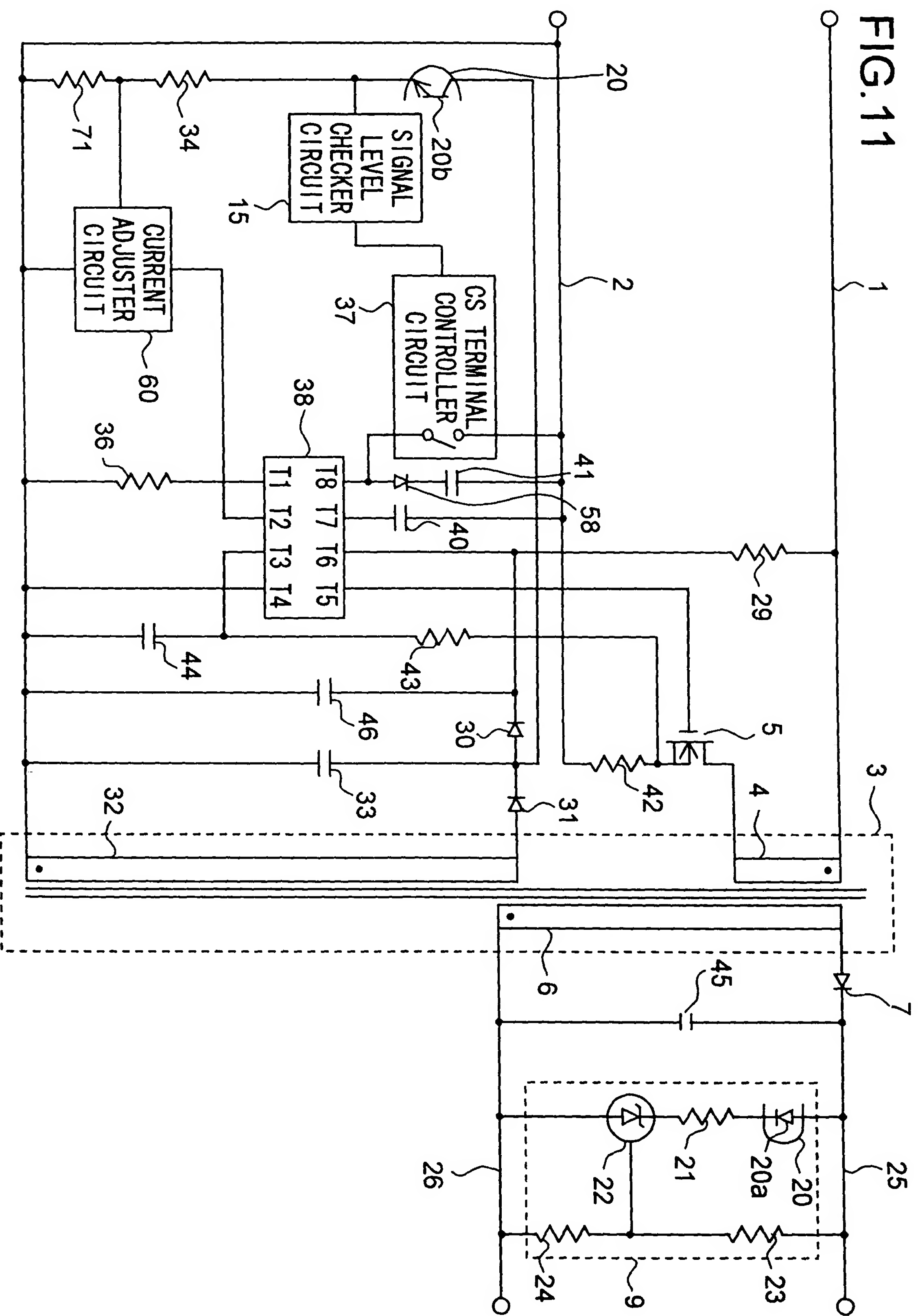


FIG.12

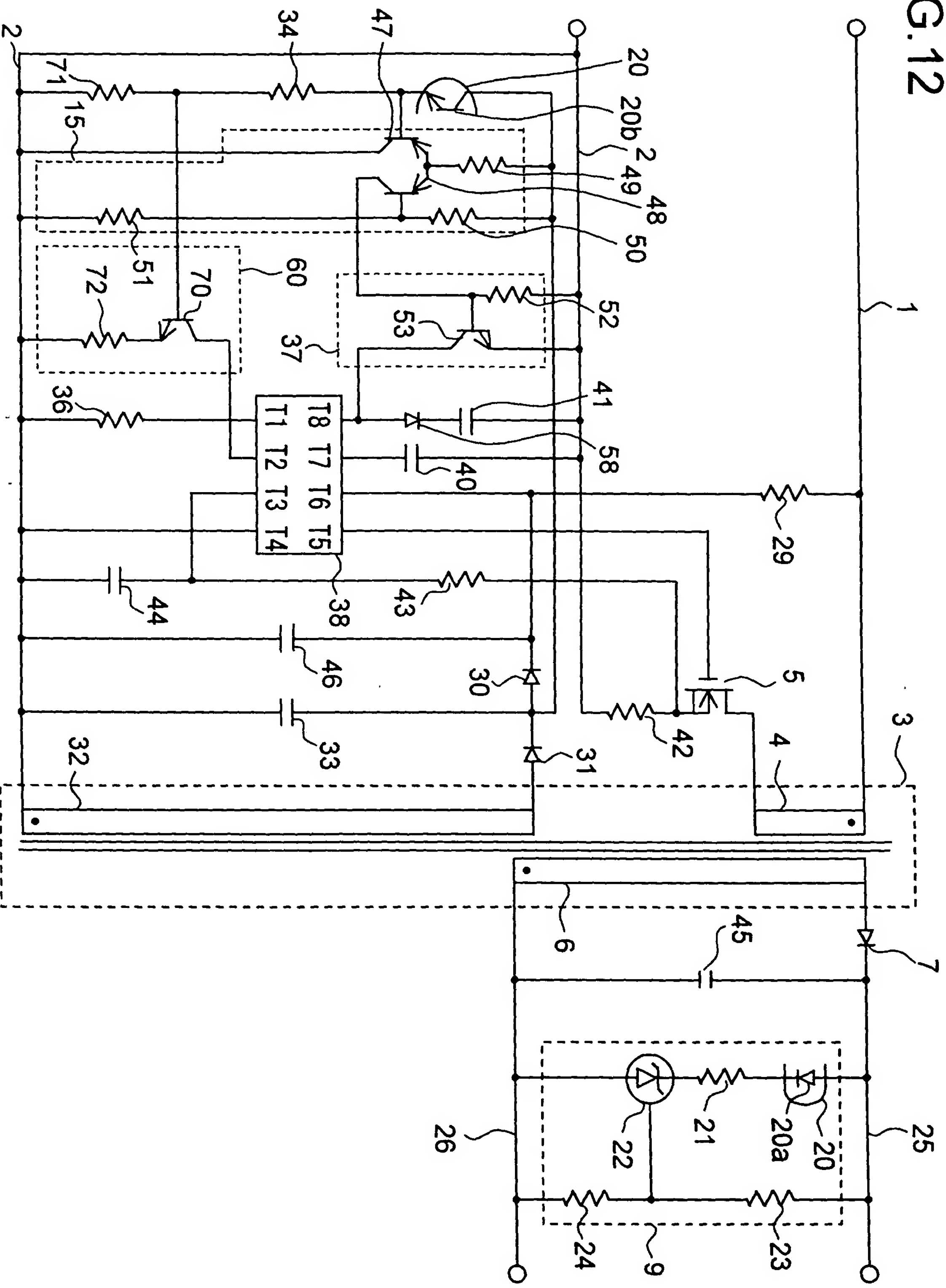


FIG. 13

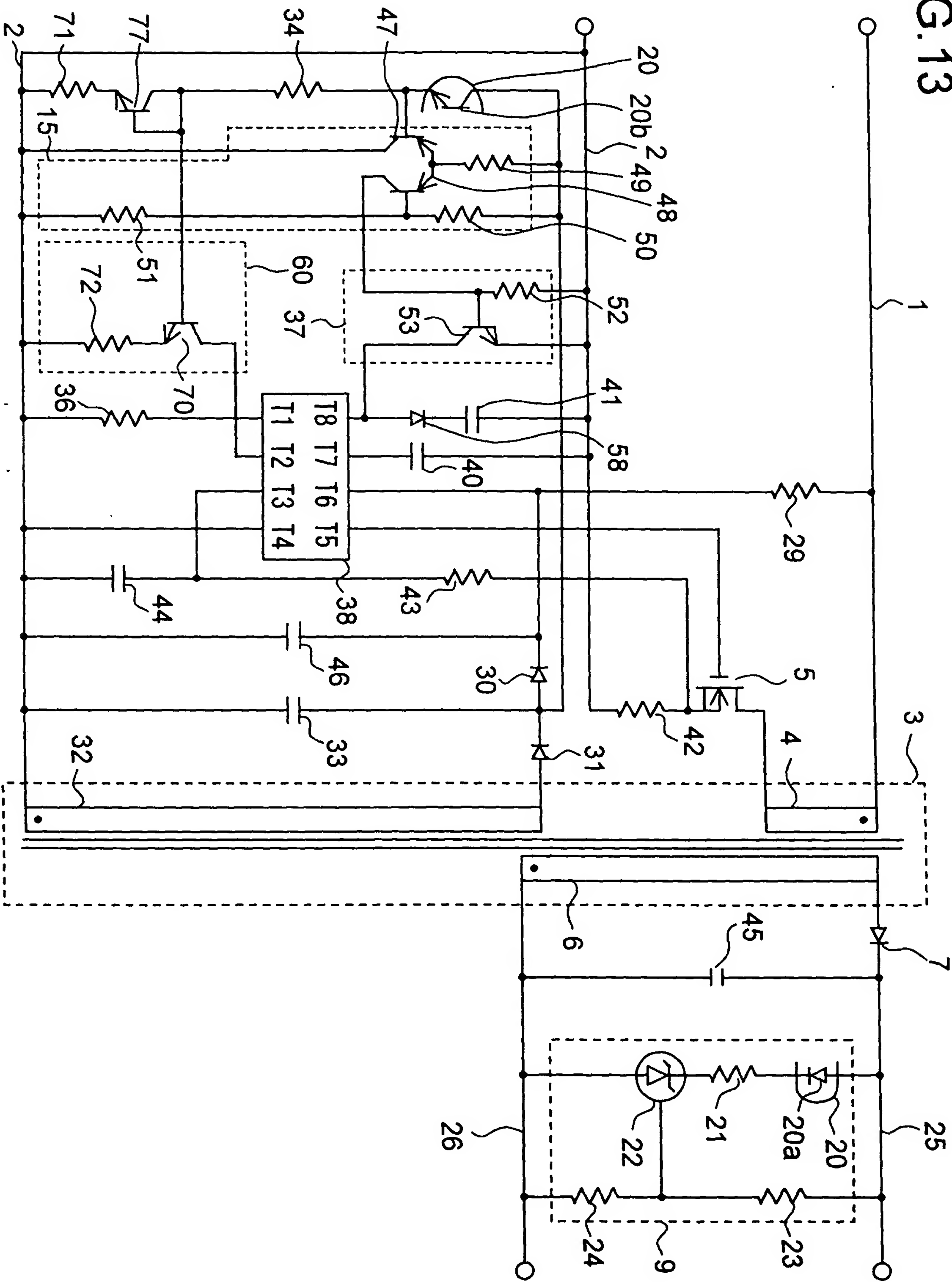


FIG. 14

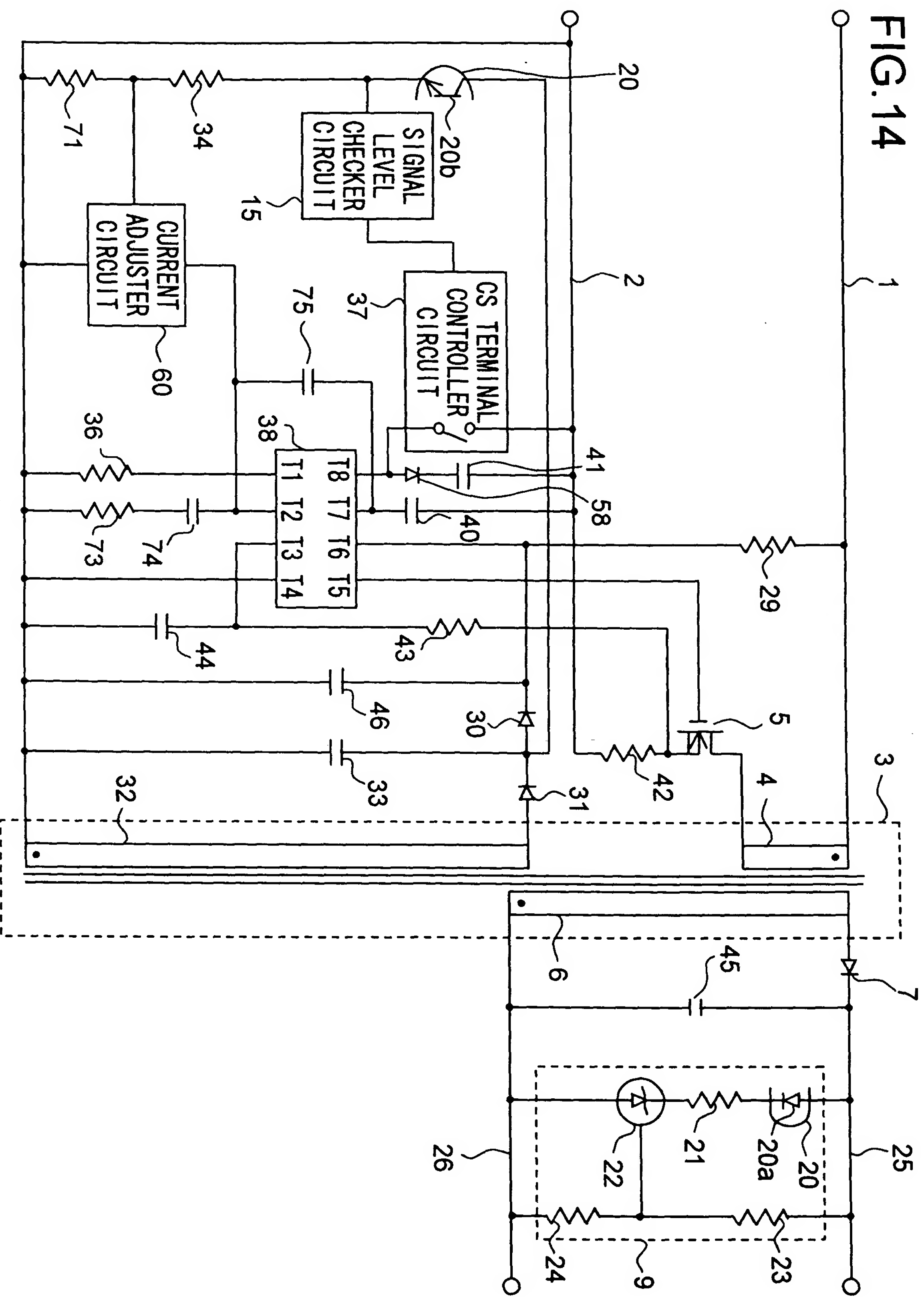


FIG. 15

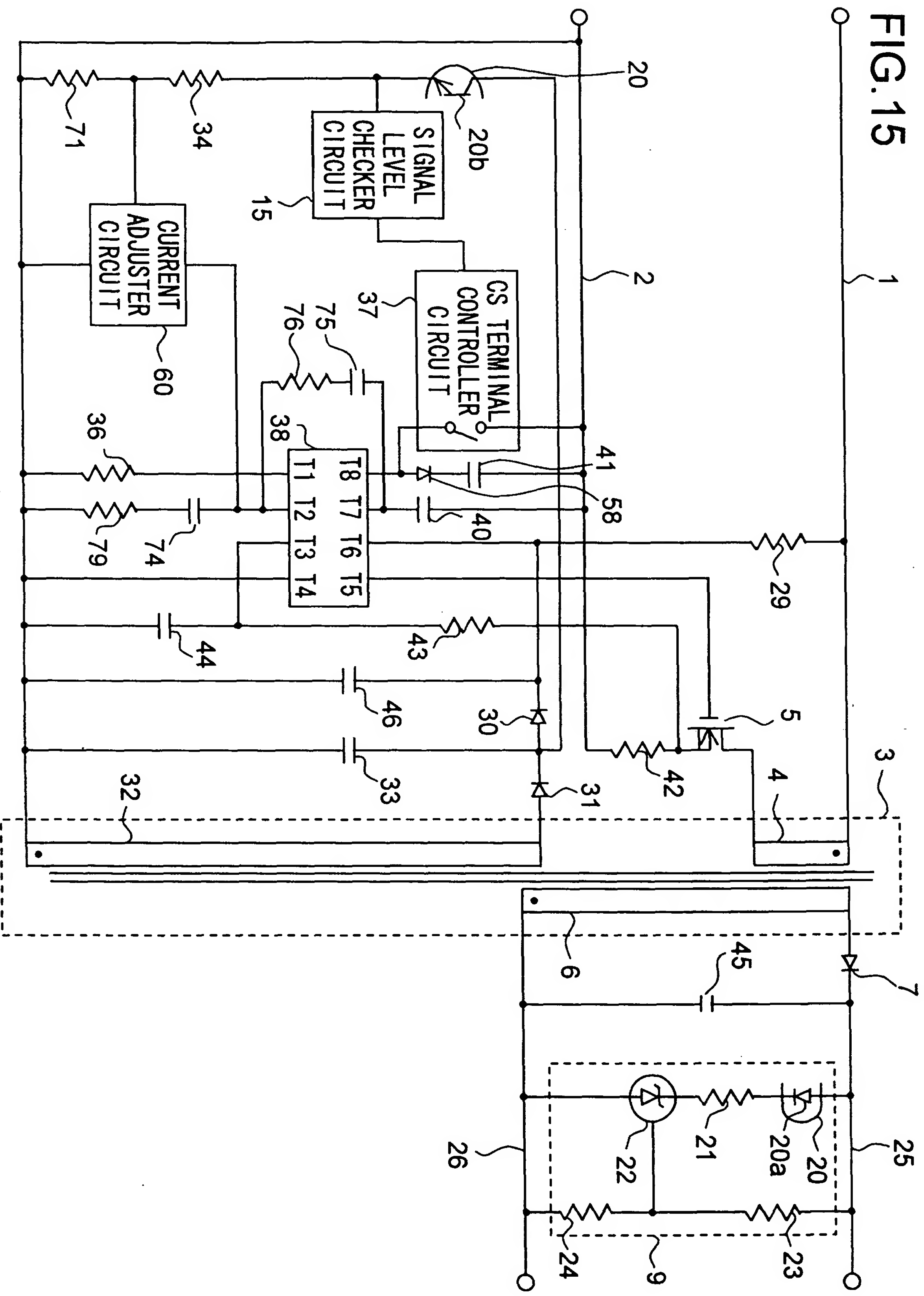


FIG. 16

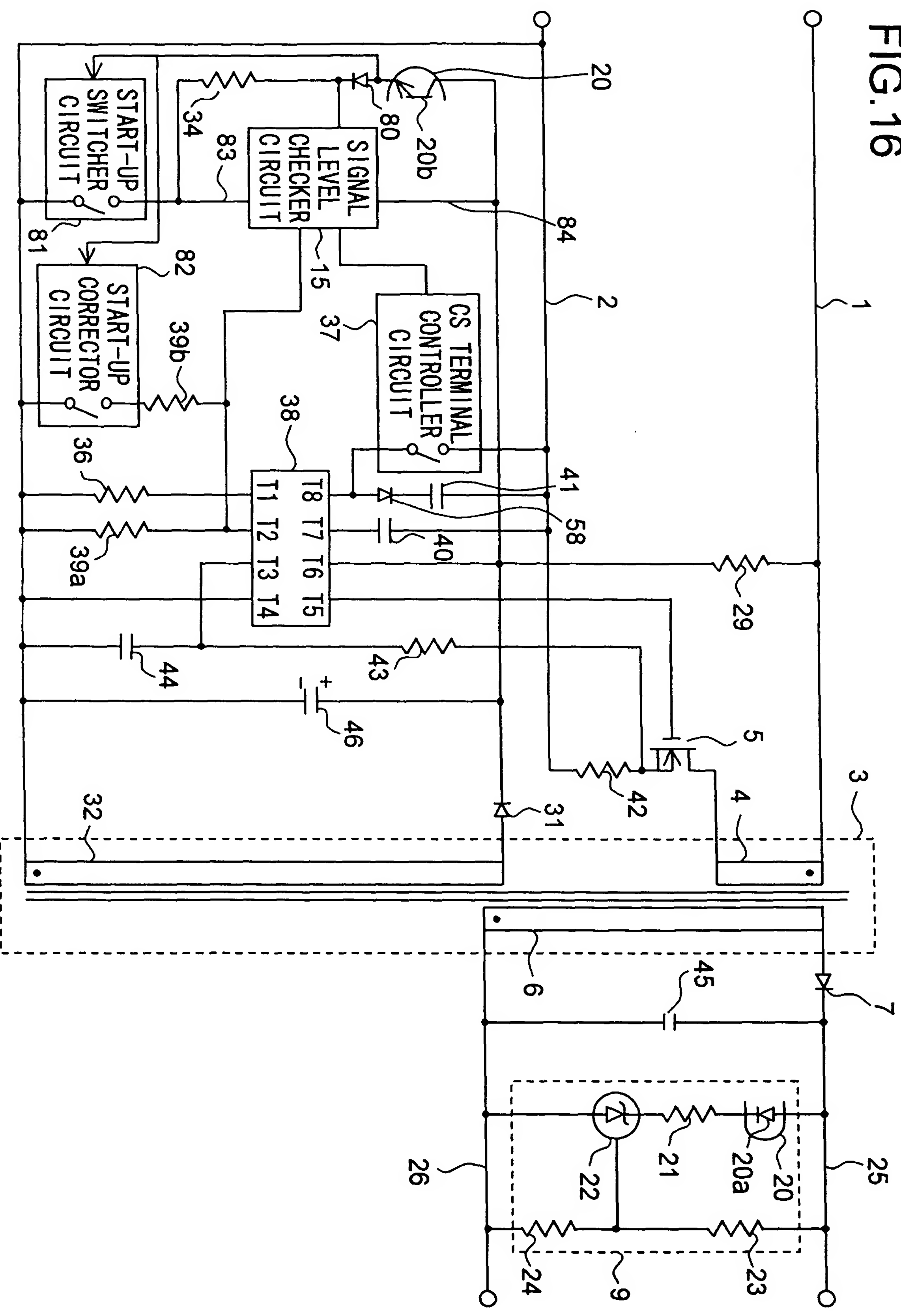


FIG.17

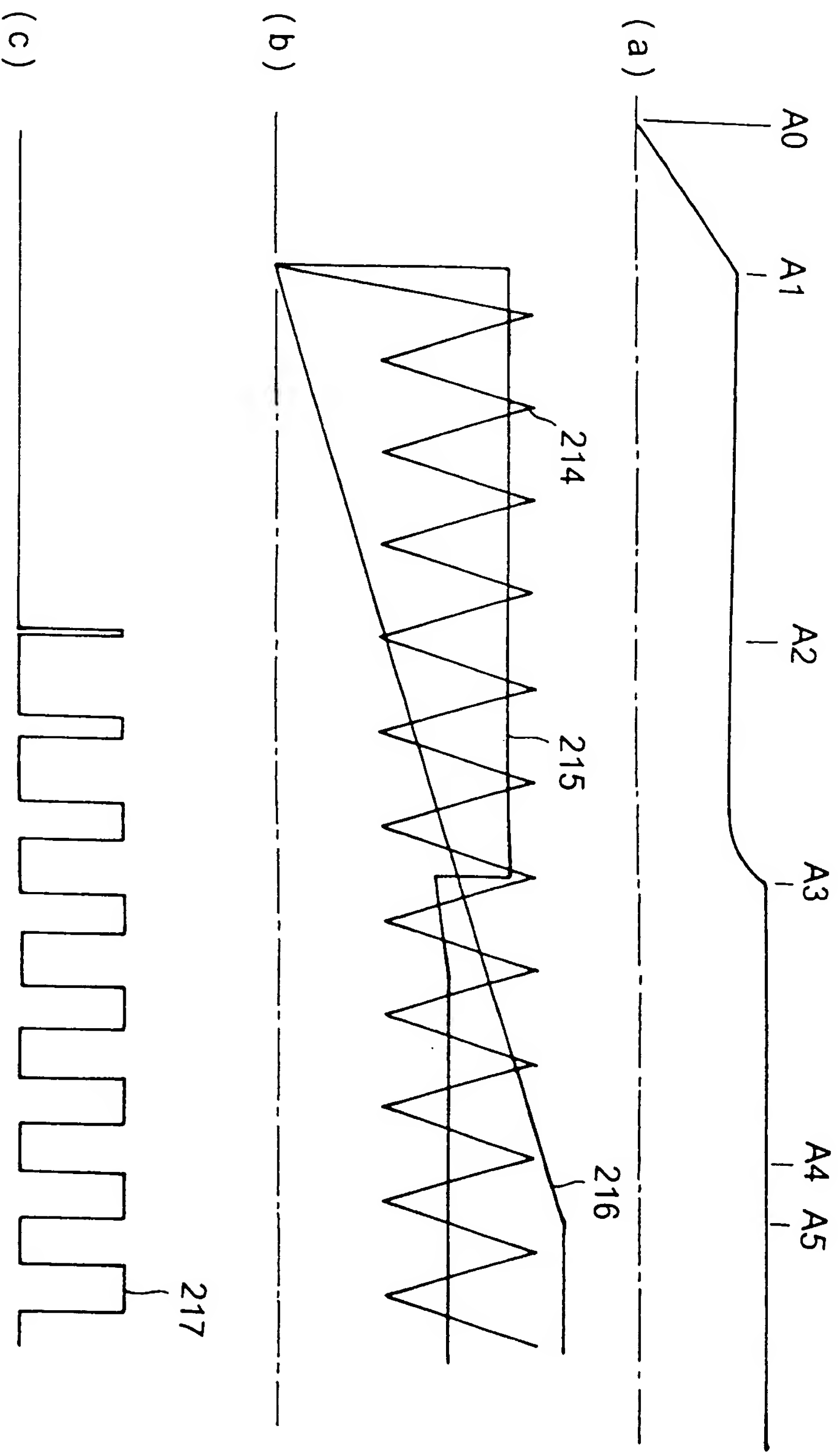


FIG. 18

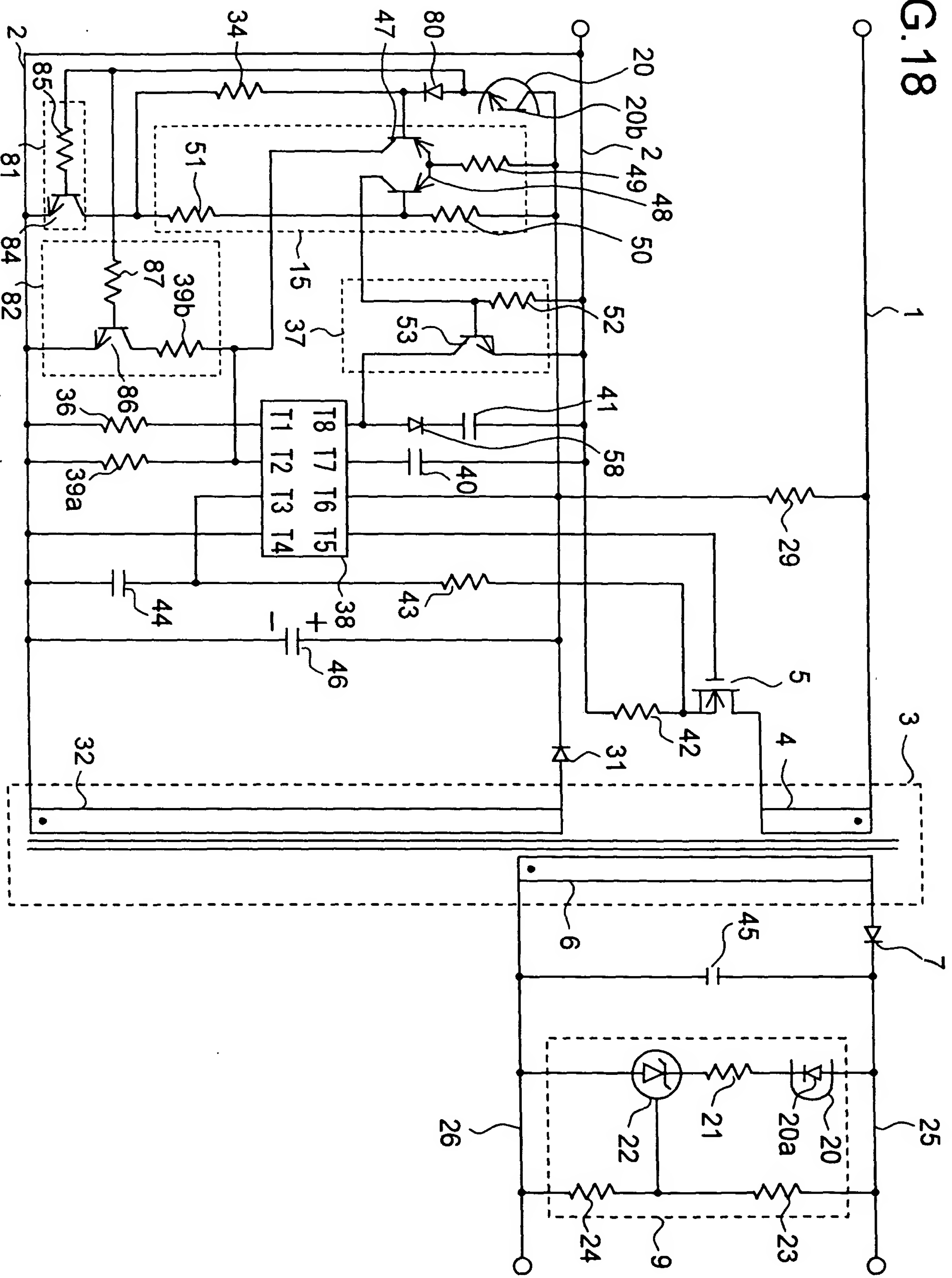


FIG. 19

The diagram illustrates a complex electronic circuit, likely a control system or a signal processor. It features several interconnected blocks and components:

- Input and Feedback Paths:** The circuit has multiple input and output terminals. A feedback path is shown with a resistor (29) and a diode (31) connecting the output back to the input.
- Control and Monitoring Blocks:**
 - CS TERMINAL CONTROL CIRCUIT (37):** This block controls the system's operation, receiving input from a terminal (41) and outputting to a terminal (58).
 - SIGNAL LEVEL CHECKER CIRCUIT (83):** This block monitors the signal level, receiving input from a terminal (80) and outputting to a terminal (15).
 - START-UP CORRECTOR CIRCUIT (82):** This block corrects the start-up conditions, receiving input from a terminal (82) and outputting to a terminal (36).
- Transistors and Diodes:** The circuit includes several transistors (5, 80, 88) and diodes (31, 40, 42, 45, 46) for signal processing and control.
- Resistors and Capacitors:** Various resistors (34, 36, 39a, 39b, 42, 43, 44, 21, 22, 23, 24) and capacitors (40, 44) are used for timing, biasing, and signal conditioning.
- Logic and Timing Elements:** A logic block (38) with inputs T1, T2, T3, T4, T5, T6, T7, T8 is used for timing and logic control. A capacitor (44) is connected to the output of this block.

The circuit is divided into two main sections by a dashed line, suggesting a modular design. The left section contains the main processing and control logic, while the right section contains the input/output interface and feedback components.

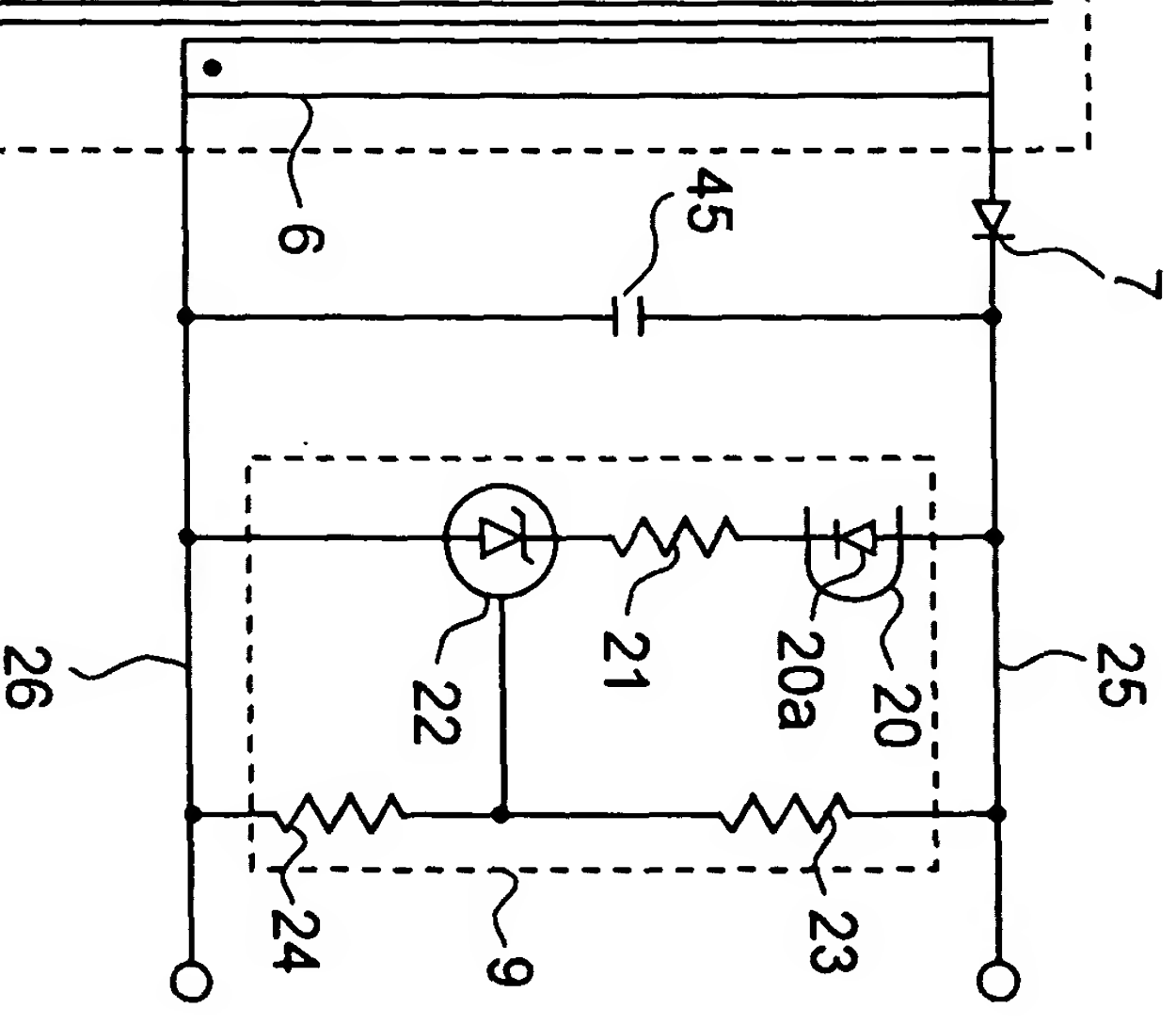


FIG.20

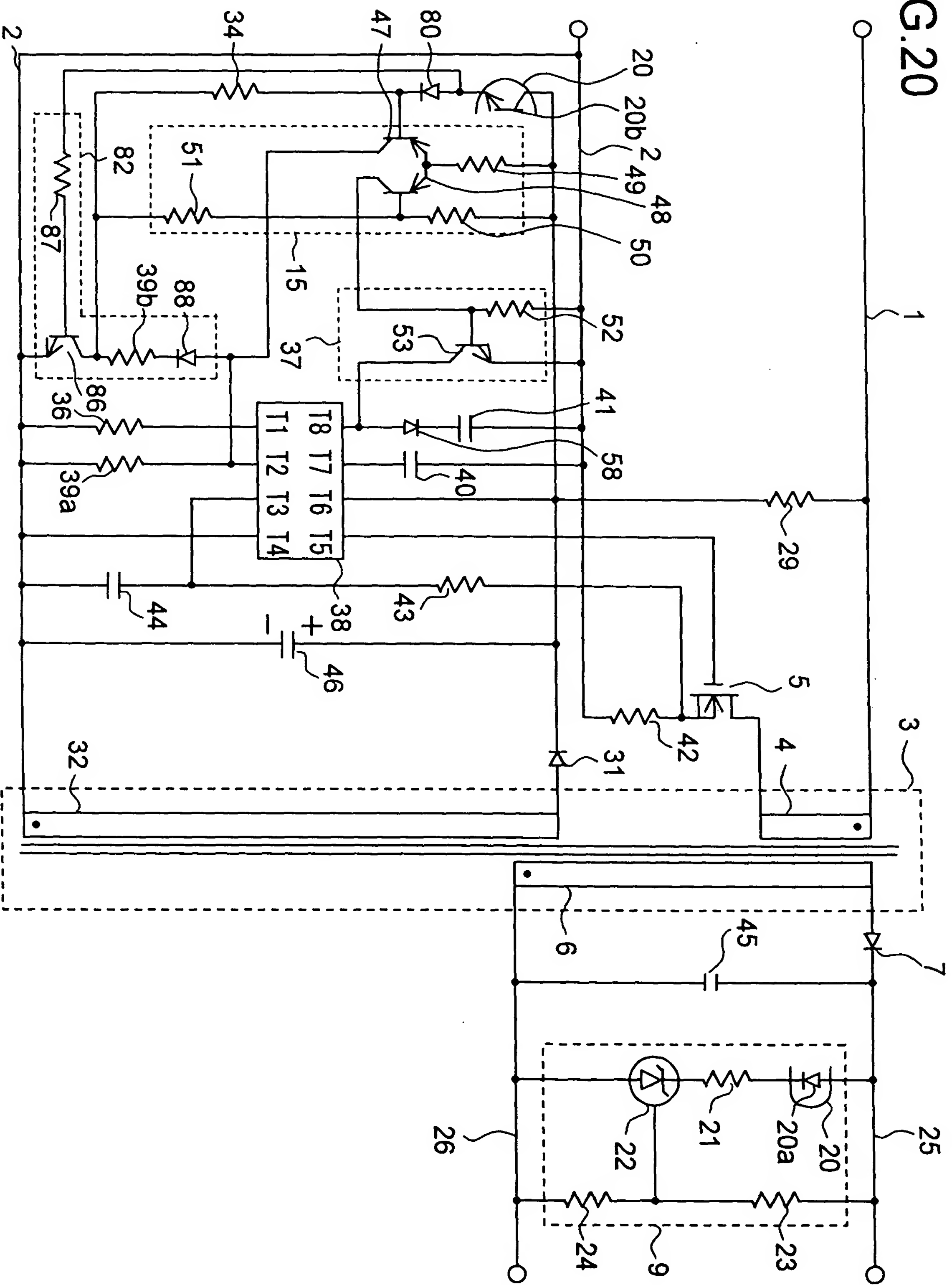


FIG.21

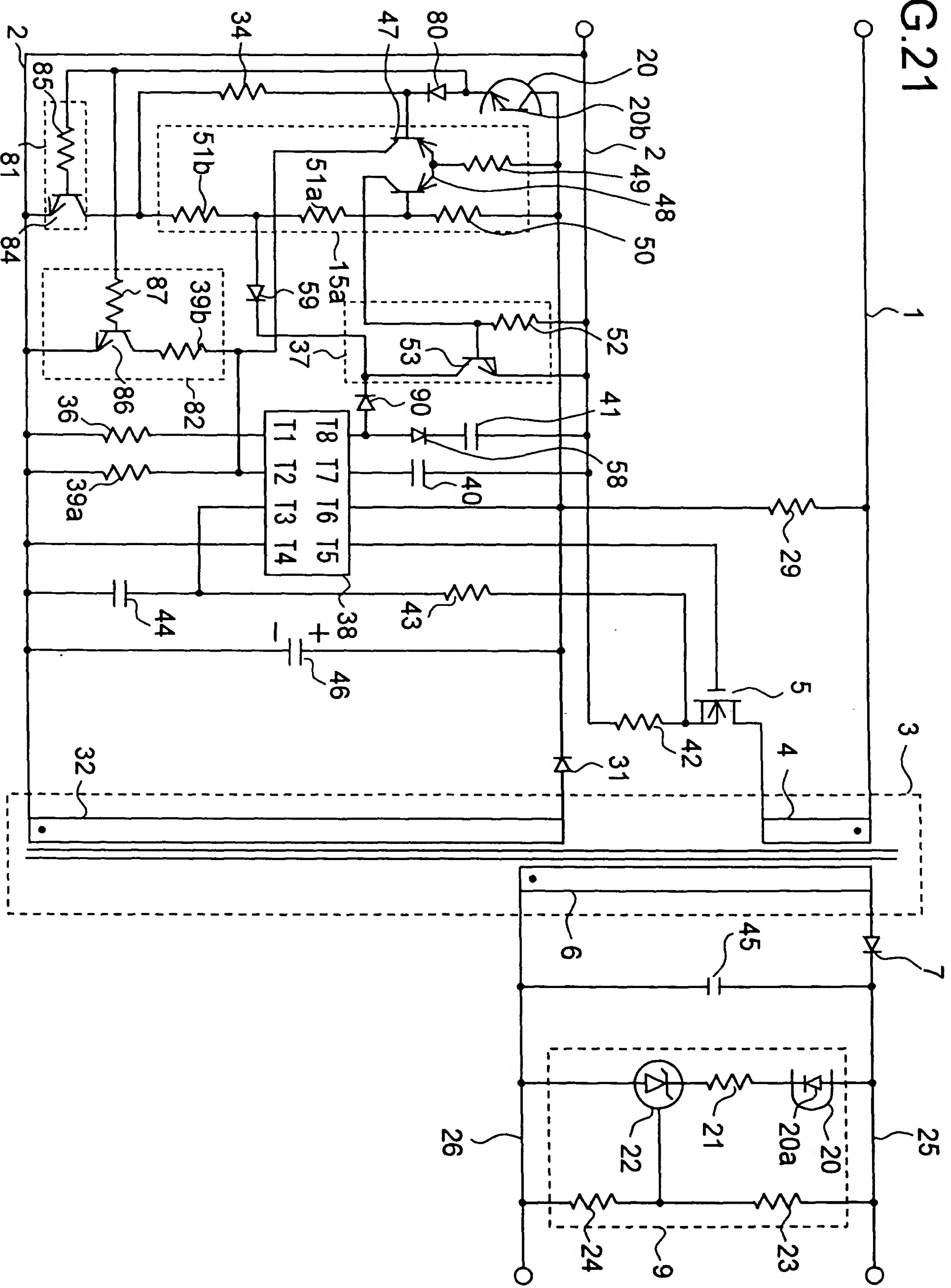


FIG.22

